Docket No: POU920010114US1

VLSI CHIP TEST POWER
REDUCTION

APPLICATION FOR
UNITED STATES LETTERS PATENT

I N T E R N A T I O N A L   B U S I N E S S   M A C H I N E S
C O R P O R A T I O N

VLSI CHIP TEST POWER REDUCTION

Field of the Invention

The present invention relates to testing of complex combinatorial and sequential logic circuits embodied in large scale integration (LSI) and very large scale integration (VLSI) circuit

5 devices and more particularly, to the reduction of power dissipation and heating of circuit elements during testing.

Background of the Invention

A fault occurring anywhere in a LSI or VLSI circuit device can have its effect propagated through a number of feedback loops including storage or memory elements in the sequential logic

10 before reaching a testable output of the device. Level sensitive scan design (LSSD) rules were devised to eliminate the complications in testing caused by this propagation through feedback loops. As described by E. B. Eichelberger and T. W. Williams in an article entitled "A Logic Design Structure for LSI Testability" on pages 462-468 of the Proceedings of the 14th Design Automation Conf., LSSD rules impose a clocked structure on logic circuit memory elements such

15 as latches and registers, and require these memory elements be tied together to form a shift register scan path so that they are accessible for use as test input and output points. Therefore, test input signals can be introduced or test results observed wherever one of the memory elements occurs in the logic circuit. Being able to enter the logic circuit at any memory element for introducing test signals or observing test results, allows the combinational and sequential logic to

20 be treated as much simpler combinational logic for testing purposes thus considerably simplifying test generation and analysis. Patents describing LSSD techniques include US. Patent No.

3,783,254; No. 3,784,907; No. 3,961,252, No. 4,513,418 and No. 5,983,380. The subject matter

of these patents and the above described Eichelberger and Williams article are hereby included by

reference.

Self-testing has been employed in connection with LSSD to reduce the volume of text

5 patterns and time it takes to generate the test patterns and to perform the testing. Self-testing

involves the use of pseudo-random pattern generators and response compression structures that

are built into logic circuit devices. Using such pattern generators and compression structures

eliminates the computer time needed to generate the tests and placing these testing elements on

the device containing the logic allows the application of vast numbers of test patterns to the

10 circuits in a high ratio and in a reasonable period of time.

In the aforementioned U.S. Patent No. 5.983,380, the shift register latches (SRLs) in the

LSSD scan paths perform both input data launching and output data capturing. The test patterns

come from the scan path that is configured into a linear feedback shift register (LFSR). The test

data is then outputted into a multiple input shift register (MISR) for data compression.

15 Alternate scan path shift cycles are applied to the SRLs exercising the combinational logic with

the contents of the SRLs and capturing the results of the response back into the SRLs where they

can be used as test inputs for the next cycle. At the end of a calculated number of cycles, the

contents of the scan path are read out as the signature to be compared with the desired value.

Such self-testing is referred to as Logic Built-In Self-Test (LBIST).

Two types of LBIST tests are applied during self test. One type is the LBIST test and another is the weighted LBIST test. As shown in Figure 1, the LBIST and weighted LBIST tests are performed sequentially with the weighted LBIST test usually following the LBIST test. One problem with this test strategy is that the AC power consumption during LBIST can be very high

5 and as more and more devices are included in the design, the heating of circuit elements will become a severe problem. There are two factors of power consumption during test. One is during the scan session where logic switching activities occurs while loading the scan chain with random patterns. The other is during the test cycle where system clocks are applied. In LBIST, the typical test patterns used make the chip function at 50% switching activity per system clock,

10 which can cause a large power supply droop during high speed testing since the power consumption is proportional to the summation of switching activities of individual devices.

Brief Description of the Invention

In accordance with the present invention, the flat LBIST and weighted LBIST test patterns are simultaneously provided different portions of the tested circuit element. This new

15 test methodology and design change achieves the same test coverage and test time as the traditional test strategy with dramatic power reduction during test. It can be applied at wafer, chip, multi chip module (MCM), and system levels of test. Most importantly, it does not need new tools for support. Current test software will work as it does with the traditional test strategy. Scheduling the LBIST and weighted LBIST tests in the same test session reduces the power

20 consumption (watts) because weighted LBIST pattern testing consumes much less power than flat pattern LBIST testing. In the same test session, if some parts of the logic is tested using weighted

LBIST while the others were tested using LBIST, the power consumed by the circuit element at any given time is reduced.

Therefore, it is an object of the present invention to provide improved LSSD testing methods and apparatus.

5   It is another object of the present invention to provide for more efficient testing of logic circuits.

It is a further object of the invention to provide improved testing procedures.

Brief Description of the Drawings

These and other objects of the invention can best be understood reading the following

10 description of the described embodiments thereof while making reference to the accompanying figures of which:

Figure 1 is a schematic diagram illustrating a prior art LBIST/weighted LBIST process;

Figure 2 is a schematic diagram of a VSLI logic chip with SRLs arranged in a LSSD chain;

15   Figure 3 is a schematic diagram of the SRL latches in the LSSD chain of Figure 2;

Figure 4 is a schematic diagram of a LBIST test circuit capable of performing both LBIST and weighted LBIST testing;

Figure 5 is a diagram of a circuit chip for performance of LBIST tests in accordance with the present invention;

Figure 6 is a flow diagram of computer testing of the chip of Figure 5 in accordance with the present invention;

Figure 7 is a diagram of a multi-chip module;

Figure 8 is a flow diagram of computer testing of the module of Figure 7 in accordance

5   with the present invention; and

Figure 9 is a block diagram of a computer testing set up.

Detailed Description of the Invention

Figure 2 shows that in accordance with LSSD rules, shift register latches (SRL's) 200 on

a semiconductor chip 202 are joined together to form a shift register LSSD scan latch chain 204

10 to facilitate testing of combinational logic blocks 206, 208 and 210 interconnected by the SRLs

200 of the scan latch chain 204. During circuit operation data is inputted to the combinational

logic blocks 206, 208 and 210 and the SRLs 200 in a parallel through the primary inputs (PIs) 212

of the chip 202 and data is outputted from the combinational logic blocks 206, 208 and 210 and

the SRLs 200 in parallel through the primary outputs (POs) vectors 214 of the chip 202. During

15 testing, the scan chain latch circuits 204 can also be loaded serially. Serial input (SRI) 216

provides a serial input to the scan chain latch circuits 204 and serial output (SRO) 218 provides

an output from scan chain latch circuits 204. Scanning inputs into the serial input SRI 216 and

out serial input 218 enables testing the SRLs 204 independently of the combinational logic 206,

208 and 210. It also allows each of the individual SRLs to be used as a pseudo-primary input or a

20 pseudo-primary output for a combinational logic block 206, 208 or 210. The logic circuits in

each of the logic blocks to be tested separately of circuits in other of the logic blocks. (While a

single scan latch chain is shown here, it should be understood that it applies equally as well to latches arranged in multiple scan chains on the chip.)

Figure 3 shows a more detailed view of a LSSD scan chain circuit 300. This chain circuit comprises a plurality of shift register latches (SRLs) 300 (herein designated as SRL_1, SRL_2, ...,

5   SRL_{N-1}, SRL_N) in which each SRL 300 includes a master latch 308 and a slave latch 310. For transfer of data between the latches and combinatorial logic 206, 208 and 210 shown in Figure 1, each of the SRLs 300 contains a data input terminal 302 from combinatorial logic circuits and a data output terminal 304 to the combinatorial logic circuits. In addition, data can be introduced into the latches at shift register input (SRI) terminal 316 and transferred from one SRL to another

10   to the shift register output (SRO) terminal. As described below, data is clocked into each SRL 300 by applying a clock pulse to master latch 308, and data is clocked out of each SRL 300 by applying a clock pulse to slave latch 310. Data is output from slave latch 310 to a succeeding master latch 308. For this purpose, the operation of the LSSD scan chain 320 is controlled by scan clock signals on the a-clk, b-clk and c-clk lines. Serial loading of the master latch 308a from

15   the SRL 116 occurs upon generation of an a-clk pulse on a-clk line. The a-clk pulse on a-clk line causes serial input applied to the SRLs 300 to be inputted to each master latch 308. Application of a b-clk on b-clk line causes data to be output from the SRLs via slave latches 310. The continuous, alternating application of a-clk and b-clk clock pulse signals on the a-clk and b-clk lines respectively sequentially propagates a data signal applied to SRI terminal 316 through scan

20   chain 320 to SRO terminal 318. To effect a parallel load, a c_1-clk block pulse is applied to c_1-clk line. This causes a parallel load of data via parallel data inputs 302 and combinational logic to each master latch 308 of the SRLs 300. Application of a b-clk or c_2-clk pulse to the b-clk line

causes a parallel output of data from each slave latch 310 of SRLs 300 to provide data on respective parallel output data lines 304.

As previously mentioned, self-testing is employed in connection with LSSD to reduce the time it takes to generate the test patterns and to perform the testing. Self-testing involves the use

5 of pseudo-random pattern generators and response compression structures that are built into logic circuit devices. Using such pattern generators and response compression structures eliminates the computer time needed to generate the tests while placing these testing elements on the device containing the logic allows the application of vast numbers of test patterns to the circuits in a reasonable period of time. Figure 4 shows a typical configuration for a logic built-in self test

10 (LBIST) circuit 400, shown in the above mentioned Molika U.S. Patent #5,983,380. In that LBIST circuit, SRLs in the SRL chains 402 perform both input data launching and output data capturing. The test patterns come from a scan path that is configured into a linear feedback shift register (LFSR) 404. The test data is then outputted into the multiple input shift register (MISR) 406 for data compression. Channel weighting logic 408 enables the performance of weighted self

15 test patterns.

During either LBIST and weighted LBIST tests, alternate scan path shift cycles are applied to the SRLs exercising the combinational logic with the contents of the SRLs and capturing the results of the response of the combinational logic back into the SRLs where they are used as the test inputs for the next cycle. At the end of the requisite number of cycles the

20 contents of the scan path is read out as the signature to be compared with the desired value. The use of pseudo random test patterns in this manner generally ensures that the circuit chip will

POU920010114US1   7

operate properly, but the applied test patterns do not properly test all logic paths on the chip. In the past, to increase the application of the testing procedure to more logic paths, the LBIST test has been followed by the weighted LBIST test as shown in Figure 1. The above mentioned Molika et al patent describes the weighting structures used in weighted LBIST testing. As

5   pointed out above, as operational speed and circuit density of chips have increased, heating of the circuit elements during LBIST testing has become a serious problem. In LBIST testing, chips are run at 1.2 times their rated operational speed to assure proper operation.

In accordance with the present invention, heating of the tested object is reduced. The LBIST and weighted LBIST tests are scheduled differently than that shown in Figure 1 to reduce

10 power consumption levels while the time it takes to perform the tests and the energy used remains the same. The invention is applicable at the chip multi chip module, and system levels of testing. As shown in Figure 5, a circuit chip 500 is provided with multiple cores and each core contains its own LBIST test structure like the one shown in Figure 4. As shown in Figure 6, as one test structure 502 runs the LBIST test using the flat pseudo-random test pattern, the other test

15 structure 504 runs the weighted LBIST test using the weighted LBIST test patterns (step 602) are tested using LBIST testing patterns while the others are using weighted LBIST under the power constraints. After that, the flat pseudo-random LBIST test patterns are applied to the test structure 504, that have been previously tested using the weighted LBIST test patterns, and the weighted LBIST test patterns are applied to the structure 502 that have been previously tested

20 using flat LBIST test patterns. During steps 602 and 604, the weighted LBIST test patterns are selected to maintain power levels below the desired maximum level. Thereafter, weighted LBIST with different weights can be applied simultaneously to both list structures 502 and 504 of the

chip (step 606). This approach takes the advantage of lower power consumption during weighted

LBIST were much less switching activities occur during test.

This test methodology will guarantee the test coverage and has no impact on test time.

But the power consumption will be reduced dramatically. Roughly, average a 30% - 40% power

5 reduction can be achieved depending on which weight is chosen and an assumption of half of the

total cores running LBIST and the other half running weighted LBIST. More power reduction is

achievable if more cores are used and, at any given time, less cores run LBIST using the flat

pseudo-random patterns while more cores run weighted LBIST using the weighted test patterns.

In any case, the average power can be calculated as follows:

$$P = \frac{1}{2} * V_{dd}^2 * f_{clk} * (A_1 * C_1 + A_2 * C_2 + ... + A_n * C_n)$$

where: V_{dd}, is the power supply voltage; f_{clk}, the clock frequency; A_1, A_2.., A_n, are the average

number of transitions (switching factor) per clock cycle on net I through n, and C_1, C_2, ..., C_n,

are the capacitances of net I through n.

Assuming the above described two core design where one core runs LBIST and the other

15 run weighted LBIST. For the LBIST test using a flat random pattern, assume the average power

consumption is 1 (0.5 for each core). For weighted LBIST test, assume the other core runs 1/16

the LBIST flat pseudo pattern 0.5 x 1/8. Then the total average power for the present

methodology is $0.5 + 0.5 \times 1/8 = 0.5625$. Therefore, more than a 40% power reduction is achieved.

As shown in Figures 7 and 8, the present invention can be used in testing a multichip module (MCM) 700 where some of the chips 702 to 708 run flat LBIST test patterns while others

5   run weighted LBIST test patterns. In step 802 of Figure 8, all 4 chips are tested as described in connection with steps 602 and 604 of Figure 6. Then in step 804, all chips run weighted LBIST tests as described in connection with step 606 of Figure 6. Therefore, power consumption can be reduced at all levels of self test. Another factor of the power reduction using this method occurs during pattern scanning where much less switching activity occurs than during the standard

10   LBIST method.

The above testing procedure provides

1.   No impact on test time;

2.   No impact on fault coverage;

3.   No new requirement on tool support;

15   4.   Compatible with existing structural LBIST base (STUMPS);

5.   Implementation is relatively simple and requires low circuit overhead.

As shown in Figure 9, the testing algorithm to test a chip 900 can be provided to the testing computer 902 on magnetic or optical media 904. A simple control logic switch 906 is

provided to respond to separate control signals for LBIST and weighted LBIST tests. Usually these signals come from the scannable General Purpose Test Register (GPTR) latches.

Above one embodiment of the invention has been described. However, it should be understood that the invention is not limited to the disclosed embodiment but includes all changes

5   that can be made in that embodiment without departing from the spirit and scope of the appended claims.